µPD7227 LCD Controller/Driver

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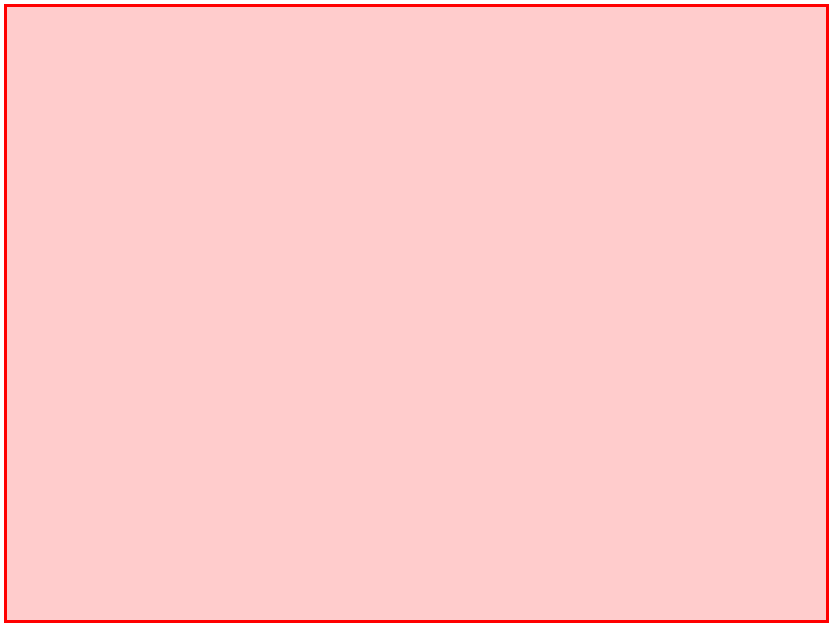
This is a datasheet of the PD7227 based on various sources of documentation for the µPD7227 LCD controller/driver chip. It features pinout and full command reference among other things.
NOTE: This datasheet is currently incomplete!

Features

- Direct LCD drive
- 8 time-sharing (single/multi-chip)
- 16 time-sharing (multi-chip)
- Expandable multi-chip display
- 5x7 character generator
- 8-bit serial I/O
- CMOS

Pinout (top view)



Block diagram

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Pins

SI — Inputs serial commands and data.

SO/$\overline{\text{BUSY}}$ — This pin functions not only as serial output (SO) but also as the BUSY signal that permits and inhibits serial data transfer.
(more to be added)

$\overline{\text{SCK}}$ — This pin inputs the serial clock that shifts the contents of the serial register, latches a signal from the SI pin and outputs serial data on the SO pin.

C/$\overline{\text{D}}$ — Specifies if the incoming serial data is a command or data. When high (command), the BUSY function of the SO/$\overline{\text{BUSY}}$ terminal is selected. When it's low (data) the SO function is selected.

Operating mode	C/$\overline{\text{D}}$	SO/$\overline{\text{BUSY}}$	SI
Write, AND, OR and Character modes	0	SO	Data input
	1	$\overline{\text{BUSY}}$	Command input
Read mode	0	SO	Invalid
	1	$\overline{\text{BUSY}}$	Command input

SYNC — This pin performs the wire-OR operation to increase the number of multi-chip display digits. When multiple chips are being used, one of the chips is selected as the master chip and the SYNC pin of the master is used as output and on as input on the slaves. The SMM (Set Multiplexing Mode) is used to configure this.

$\overline{\text{CS}}$ — Chip select signal. When this is low, the serial communication is enabled.

C_0 - C_{39}	Column outputs to the LCD.
R_0 - R_{15}	Row outputs to the LCD.
V_{LC1} - V_{LC4}	LCD drive voltage input pins that generate the LCD drive signals (C_n and R_n).
RESET	High active reset pin.
CLOCK	External clock input. When multiple chips are configure, a clock signal with the same frequency and phase should be used for all the chips.
V_{DD}	Positive power supply.
V_{SS}	Ground.

Commands

Here's a summary of the available commands. Detailed information on the commands is available below.

Bits								Hex	Command	Description
7	6	5	4	3	2	1	0			
0	0	0	1	0	F_2	F_1	F_0	10-17	Set Frame Frequency	Sets the frame frequencies.
0	0	0	1	1	M_2	M_1	M_0	18-1F	Set Multiplexing Mode	Sets time-sharing count, row driver function, memory bank and SYNC port function.
0	0	0	0	1	0	0	E	08-09	Display On/Off	Sets if the display should be enabled or not.
0	1	1	0	0	0	P_1	P_0	60-63	Set Read Mode	Sets read mode.
0	1	1	0	0	1	P_1	P_0	64-67	Set Write Mode	Sets write mode.
0	1	1	0	1	0	P_1	P_0	68-6B	Set OR Mode	Sets OR mode.
0	1	1	0	1	1	P_1	P_0	6C-6F	Set AND Mode	Sets AND mode.
0	1	1	1	0	0	1	0	72	Set Character Mode	Sets character mode.
0	1	0	B_2	B_1	B_0	P_1	P_0	40-5F	Bit Set	Sets the bits specified by B_0 - B_2 at the data pointer.
0	0	1	B_2	B_1	B_0	P_1	P_0	20-3F	Bit Reset	Clears the bits specified by B_0 - B_2 at the data pointer.
1	B	D_5	D_4	D_3	D_2	D_1	D_0	80-FF	Load Data Pointer	Loads the immediate data pointer where D is the address and B is the memory bank.

P_1	P_0	Data pointer operation
0	0	The pointer is incremented by 1 every time data is input/output.
0	1	The pointer is decremented by 1 every time data is input/output.
1	0	---
1	1	No change.

Set Frame Frequency (SFF)

Sets the frame frequencies. The frame frequencies are obtained by demultiplying the clocks input from the CLOCK pin by the demultiply rates specified by bits F_2 through F_0.

F_2	F_1	F_0	Frame frequency
0	0	0	$fcl/2^{14}$
0	0	1	$fcl/2^{13}$
0	1	0	$fcl/2^{12}$
0	1	1	$fcl/2^{11}$
1	0	0	$fcl/2^{10}$

fcl is the clock frequency.

Set Multiplexing Mode (SMM)

Specified the time-sharing count, the I/O operation of the SYNC pin and data memory banks (effective only for the 8 time-sharing specification). This command also selects the row driver functions.

M_2	M_1	M_0	Time-sharing count	Row driver function	SYNC pin	Memory bank
0	0	0	8	ROW0-ROW7	Input	Bank 0
0	0	1				Bank 1
0	1	0			Output	Bank 0
0	1	1				Bank 1
1	0	0	16	ROW8-ROW15	Input	Banks 0 and 1
1	0	1				
1	1	0		ROW0-ROW7	Output	
1	1	1				

Display Off (DISP OFF)

Erases the LCD display indicating the relationship between the row and column signals regardless of the data in memory.

Display On (DISP ON)

Displays data according to the data in memory.

Set Read Mode (SRM)

Sets read mode and data pointer operation. Every time data is read the contents of the memory addressed by the data pointer is loaded to the serial register.

Set Write Mode (SWM)

Sets write mode and data pointer operation. This mode writes serial data directly to the memory addressed by the data pointer.

Set OR Mode (SORM)

Sets OR mode and data pointer operation. The serial data is ORed with the contents of the memory addressed by the data pointer and stored at the same address.

Set AND Mode (SANDM)

Sets AND mode and data pointer operation. The serial data is ANDed with the contents of the memory addressed by the data pointer and stored at the same address.

Set Character Mode (SCM)

Sets character mode. In this mode, the serial data is sent to the character generator which writes a 5x7 character into memory. The data pointer is incremented by 5 each time.

Bit Set (BSET)

Sets the bits specified by B_0 through B_2 of the memory addressed by the data pointer. Control is returned to the previously selected mode after this command has been executed.

Bit Reset (BRESET)

Clears the bits specified by B_0 through B_2 of the memory addressed by the data pointer. Control is returned to the previously selected mode after this command has been executed.

Load Data Pointer Immediate (LDPI)

Loads the data pointer with immediate data. B specifies what bank to use.

Character table

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